Application of Fuzzy Integrated FMEA with Product Lifetime Consideration for New Product Development in Flexible Electronics Industry

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Abstract:

Purpose: the aim of this paper is to minimize the risks of new product development and shorten time-to-market, particularly for high-tech enterprise where the complexity of the product generates vast amount of failure mode.

Design/methodology/approach: first, the concept of Critical Consideration Factor (CCF) is introduced based on product-specific technical characteristics, expected lifetime, and yield requirement to identify and prioritize the critical failure mode in the subsequent Failure Mode and Effect Analysis (FMEA), followed by process characterization on the high-risk failure mode and Critical Parameter Management (CPM) practice to realize a robust mass production system of the developed technology. The application on the development of advanced flexible substrate and surface finishes fabrication technique is presented.

Findings: through the proposed methodology, the risk level of each potential failure mode can be accurately quantified to identify the critical variables. With process characterization, reliability of the product is ensured. Consequently, significant reduction in development resources and time-to-market can be achieved.

Practical implications: the development strategy allows high tech enterprises to achieve a balanced ecosystem in which value created through adaption of new technology/product can be thoroughly captured through commercialization in a timely manner with no field failure.

Originality/value: the proposed development strategy utilizes a unique approach with thorough considerations that enables high tech enterprise to deliver new product with rapid time-to-market without sacrificing product lifetime reliability, which is key to achieve competitive advantage in the highly dynamic market.

Keywords: new product development, risk management, failure mode and effect analysis, critical parameter management, advanced manufacturing, industry 4.0

1. Introduction

1.1. New Product Development

To remain sustainable and profitable, high tech enterprises face multiple challenges in competitive business environments and rapid changes in market demand. One of the key success factors is continuous investment in R&D to create value by commercializing technology into products, setting industry standards, and effectively deterring the entry of rivals (Zahra, 1996). With ever increasing customer expectations, time becomes the critical factor in the development of new technology. Manufacturers are required to achieve short development cycles and consequently time-to-market, while simultaneously offering cost advantages and scalability. Opportunities from NPD also incur huge risks, in which unpredictable obstacles can arise during mass production that lead to unstable yield loss and impede product commercialization. Managing NPD is a vital and challenging process, as it involves extensive financial and human resources (Bhuiyan, 2011). In fact, a considerable number of products never make it to the market, with a failure rate of 25% to 45% (Mosley, 1994; Crawford, 1987). Avoiding failure is paramount in the development of technical products. The earlier the failure detection, the more economic loss can be avoided (Figure 1) and the faster commercialization can be achieved (Würtenberger, Kloberdanz, Lotz & Von Ahsen, 2014). In addition to the cost, commercialized products that experience field failure during their product lifetime will negatively affect customer experience, not to mention possible liability issue. Therefore, solving these unforeseeable problems is critical to achieve successful technology transfer. Indeed, organizations need to employ a multi-dimensional development strategy to ensure that the value created is in equilibrium with the value captured (Rajan, 2016).
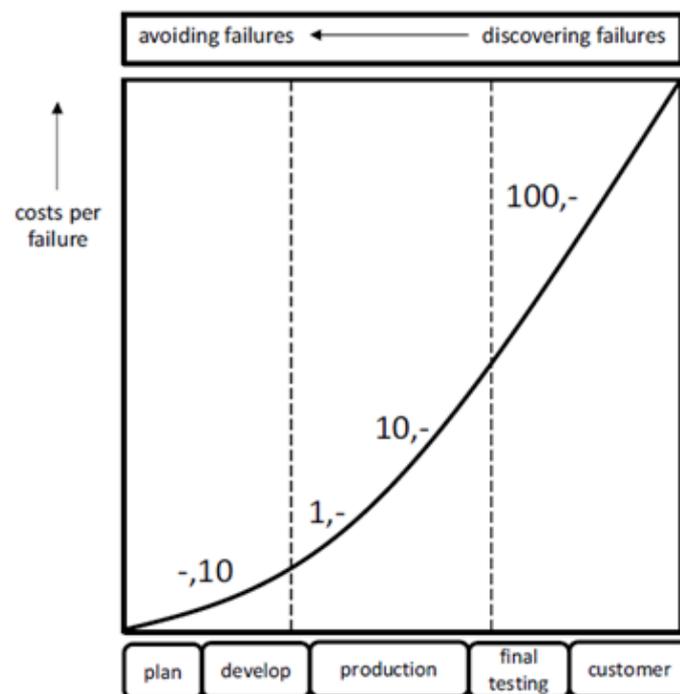

Figure 1. Cost per failure that increase logarithmically at different development stage (Würtenberger et al., 2014)

Success of the NPD process requires synergy from cross-functional teams, management support, and conducive organizational structure to achieve the desired product performance, speed to market, and development cost (Schimmoeller, 2010). Quality improvement tools, such as quality function deployment (QFD), benchmarking, conjoint analysis, and FMEA have been investigated by previous researchers. FMEA in particular, has been used in numerous development strategy frameworks. For example, Belu, Rachieru, Militaru & Anghel (2012) demonstrated the application of design FMEA with functional analysis in new product development stage.

Doğan and Cebeci (2016) integrated the use of QFD to generate FMEA based on customer requirement in NPD process. These studies, despite being able to detect possible risks beforehand, do not ensure a robust system that is ready for mass production while taking into account product lifetime reliability. Natarajan, Senthil, Devadasan, Mohan and Sivaram (2013) implemented quality and reliability on to new product development process, however the methodology presented is not quantitative as it focuses on systematically achieving certain milestone on the product development. Moreover, methodology in traditional FMEA is highly debatable due to the subjective rating as well as questionable weighting and calculation formula. Various methods have been proposed to improve FMEA such as using grey relational analysis and fuzzy logic based on safety, quality, and cost (Baynal, Sari & Akpinar, 2018; Banduka, Tadić, Mačužić and Crnjac, 2018). Therefore, there is a need for novel development strategy based on FMEA that takes into account product quality & reliability from the technical aspect through quantitative analysis to intelligently manage and optimize development resources to reduce development time.

1.2. The Flexible Electronics Industry

Increasing demand for advanced electronic products with a smaller form factor, multi-functionality, higher performance, and lower overall cost has driven the semiconductor industry to continuously innovate emerging advanced packaging technologies using flexible substrates. The electronic packaging field constitutes a highly sophisticated area that necessitates specific expertise on numerous levels. Choosing the optimal process equipment and materials, combined with innovative design solutions that address thermal, mechanical, and electrical issues will be the key success factors. Figure 2 shows the construction of an advanced electronic package with heterogeneous integration. From top to bottom, the package consists of die (integrated circuit/ IC)/component, IC level interconnect, package level interconnect (1st level), substrate, board level interconnect (2nd level), and the main board itself.
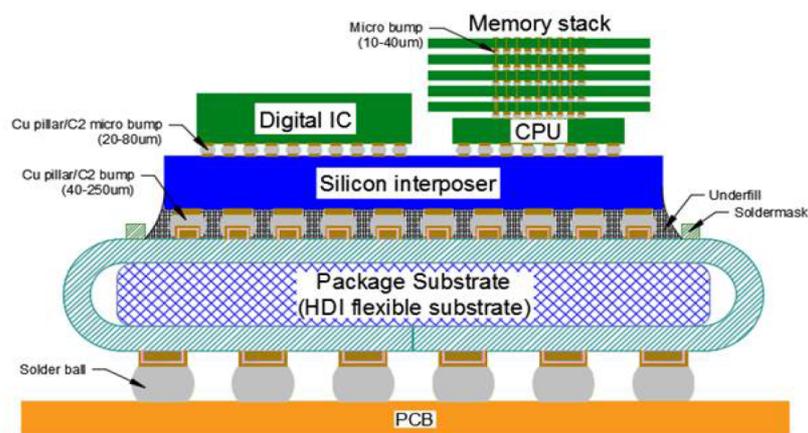

Figure 2. Heterogeneous integration in an advanced electronic package
(Pun, Islam, Rotanson, Cheung & Chan, 2018a)

With such heterogeneity in a microsystem, various components are integrated by different kinds of materials and interfaces in a compact space. The reaction between these materials and the environment determines manufacturability, functionality, and reliability. With the extant trend that is shifting towards the "More than Moore" law, 3D IC integration using through silicon via (TSV) has been developed for higher density and shorter signal propagation (Pangracious, Marrakchi & Mehrez, 2015). To enable this, packaging substrate is essential to fan out the compact circuitries between the 3D IC module and the main board, so that thermal expansion mismatch can be minimized, and a less dense main board is required (lower cost) (Lau, 2015). Moreover, scaling of silicon devices is reaching its physical limit (Nawrocki, 2010). Interconnect technology is also growing at a rapid pace (Figure 3). Therefore, diversification of semiconductor products is predicted to create new competition in advanced packaging substrates and their interconnect technologies. Advanced packaging will be the critical enabler of a wide variety of devices in many applications, such as

OLED/AMOLED, LCD/TFT displays, smart wearables, medical imaging, and hyperconnected cloud (HyCC) for the internet of things (IoTs). However, integration of more components and material interfaces on advanced package configurations, such as system-in-package (SiP), package-on-package (PoP), and 3D IC integration modules will increase potential failure modes in an exponential manner. These failure modes (especially highly critical ones) must be eliminated early during the development stage, as conducting failure analysis after product commercialization involves another set of huge resources, and often necessitates design changes and engineering change notices (ECN) on many levels due to system complexity. Furthermore, encountered field failures will incur major losses for enterprises in terms of liability, cost, reputation, etc. Therefore, product lifetime performance must constitute a top priority.
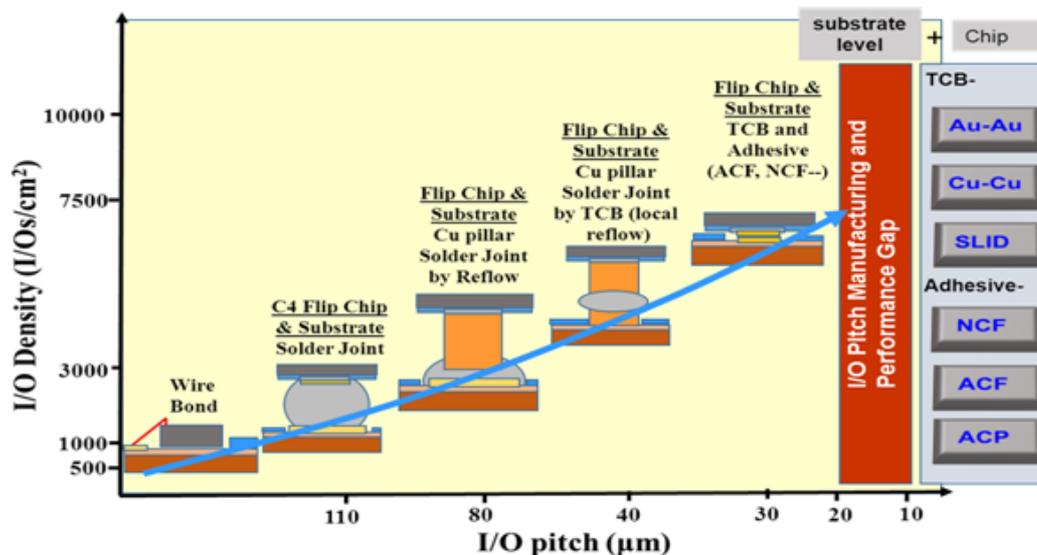

Figure 3. Trend of high-density interconnect (HDI) to support advanced package development

With the demanding product features, along with the rapid change of trend in electronics industry (Figure 4), market research is essential to ensure new product development process is targeting the relevant market segment that benefits both the consumer and organizations. Based on these emerging market trends, three main fields are identified:

1. **Display market:** Future display modules are also moving towards the integration of display driver IC and touch controller IC, which benefits design, manufacturing, size reduction, and performance (Synaptics, 2014). This integration means that more functionalities can be incorporated into a single IC, which also requires a COF (Chip-on-film) with an increasingly finer pitch. Expected product lifetime: <5 years.

2. **Medical devices market:** The medical field demands high performance reliability and ultra-compact module integration using system in package (SiP) and package on package (PoP) which involve multiple assembly processes. Such configurations necessitate advanced packaging solutions, in terms of interconnect density, pitch, and substrate line/space scalability. Expected product lifetime: 10-15 years.

3. **Hyperconnected Cloud Computing (HyCC):** In the coming IoTs (Internet of Things) era, all kinds of data will be collected, transmitted, stored, and analysed in an enormous virtual space to generate new values and finally be displayed for end users. Translating this in terms of packaging requirement, a fine line/spacing packaging substrate having short wiring between devices is needed to minimize signal propagation delay while reducing package size. Furthermore, as transmission speed is also increasing for these applications, smooth conductor roughness and low dielectric constant become essential to minimize conductor loss (skin effect) and dielectric loss, respectively. Expected product lifetime: 10-15 years.
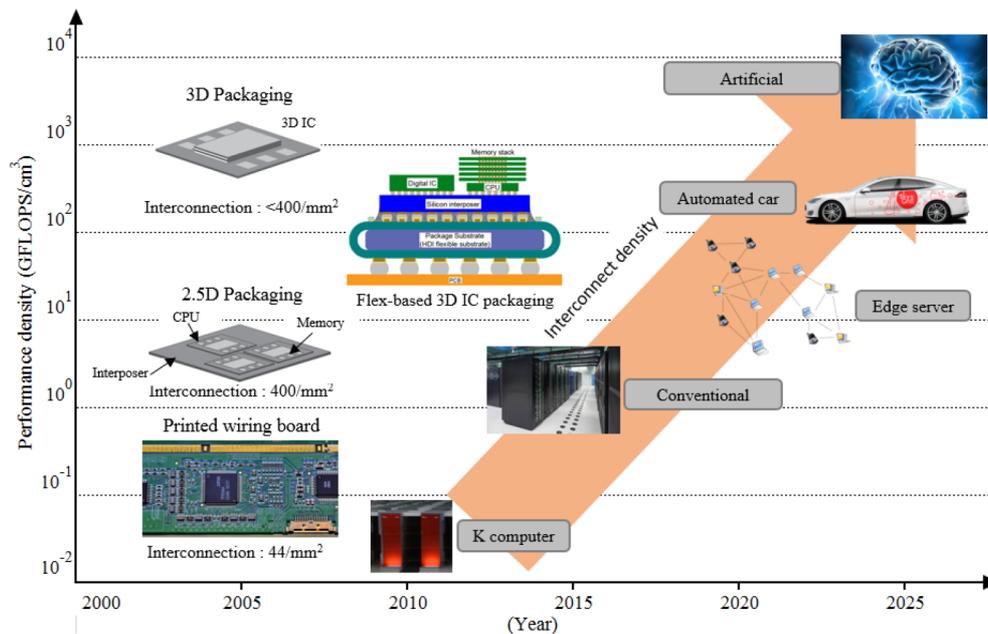
Figure 4. Device packaging technology for servers (Aoki, 2017)

1.3. Proposed State-of-the-Art Technology

Taking the existing technical challenges involved in the electronic packaging requirement in emerging products into account, the following technologies related to flexible substrate are developed:

1. **Flexible circuit fabrication with Fully Additive Process (FAP):** The substrate is an integral part of packaging, as it serves as the backbone of electronic devices by interconnecting all components mechanically and electrically. A flexible substrate is typically fabricated by a subtractive or semi-additive process (SAP or MSAP, respectively), which possesses limitations on meeting circuit density below 20 um pitch, which limit package miniaturization. A fully additive process (FAP) has been developed and proven to outperform the conventional process in terms of functional performance and overall process steps/cost.

2. **Advanced Surface Finishing with Electroless Ni/Electroless Pd/Immersion Au (ENEPIG):** Surface finish plays a vital role in the final steps of substrate fabrication since it not only protects the exposed copper circuit, but also affects the final interconnection performance due to the interfacial reaction of the surface finishing material during the assembly process. ENEPIG is a promising solution to address the reliability and miniaturization requirement of future electronics due to the low overall thickness and electroless plating method that simplifies process steps.

List of technical features to be addressed in the development of the two technologies is shown in Figure 5. Combining these two technologies in a reel-to-reel form with the latest interconnect technology constitutes a unique approach to realize an advanced electronic packaging system while achieving considerable process steps and cycle time reduction, as shown in a comparative study of our production line (Figure 6). These two technologies are promising to support advanced interconnect technologies, including direct diffusion bonding and copper pillar soldering (1st level interconnect) and low temperature soldering (2nd level interconnect).

Due to the high level of complexity and precision required on the development of the two mentioned technologies, a vast amount of technical challenges/failure mode is to be expected prior to mass production. Solving the large amount of failure modes is unrealistic due to the prolonged development time/time-to-market, which significantly deteriorates the competitiveness of high-tech enterprises. In this paper, a unique development strategy for robust technology transfer is presented and applied to the development of the new flexible electronics substrate fabrication and surface finishing technology.
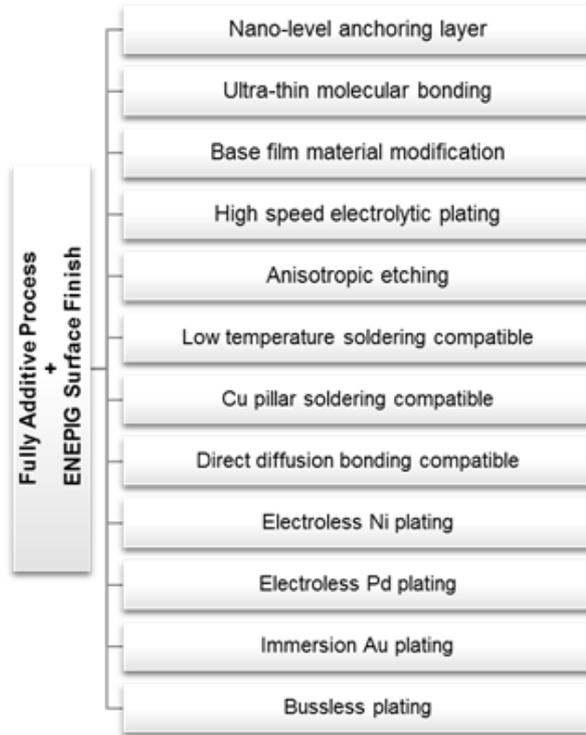
Figure 5. Features of the proposed state-of-the-art technology
in fulfilling the latest product technical requirement
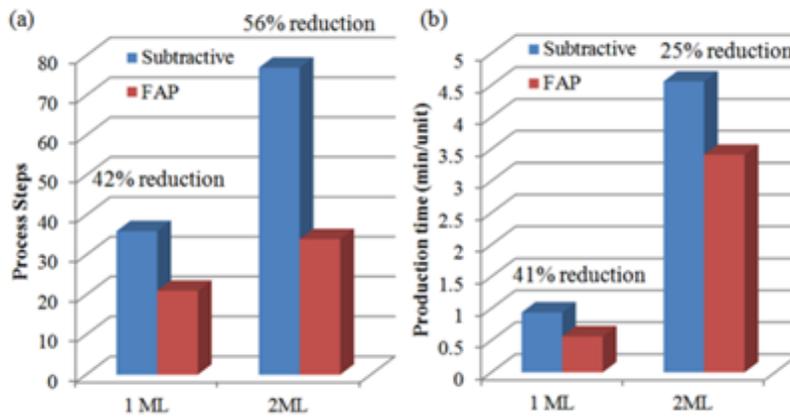
Figure 6. (a) Process steps reduction; (b) Production time reduction with the
proposed development technology as compared to conventional process

2. Proposed NPD Methodology

Figure 7 shows all the factors affecting the competitiveness of high-tech enterprise including external key drivers, relationship management, human resources, development tools, and sophisticated technology. This work focuses on the development of state-of-the-art technology and the corresponding development tools to streamline and accelerate the new technology development through a unique approach that enables NPD process with high product reliability while enhancing time to market. Figure 8 shows the steps of the proposed development tools methodology. The main key to achieve this to prevent failure occurrences earlier during the development stage through optimizations of the related variables. Critical consideration factors (CCF) are first defined based on the unique product features that are specific to the end application, with respect to technical characteristics, lifetime, and yield requirements, as shown in Figure 9.
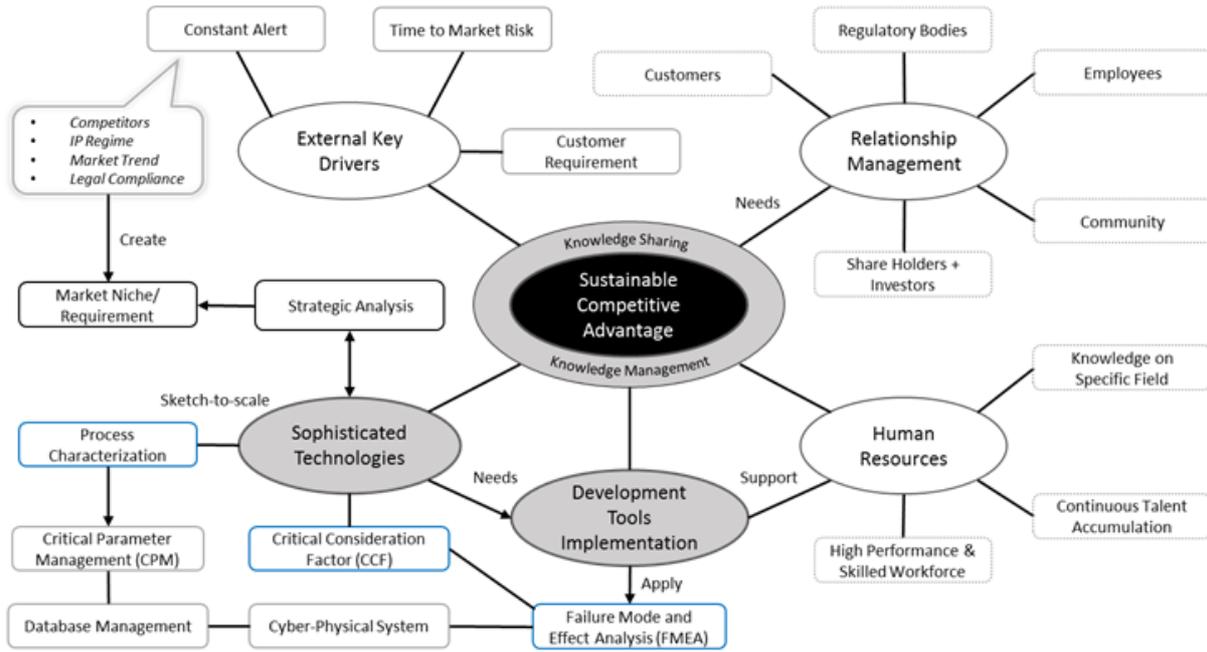
Figure 7. Factors affecting competitive advantage of high-tech enterprises
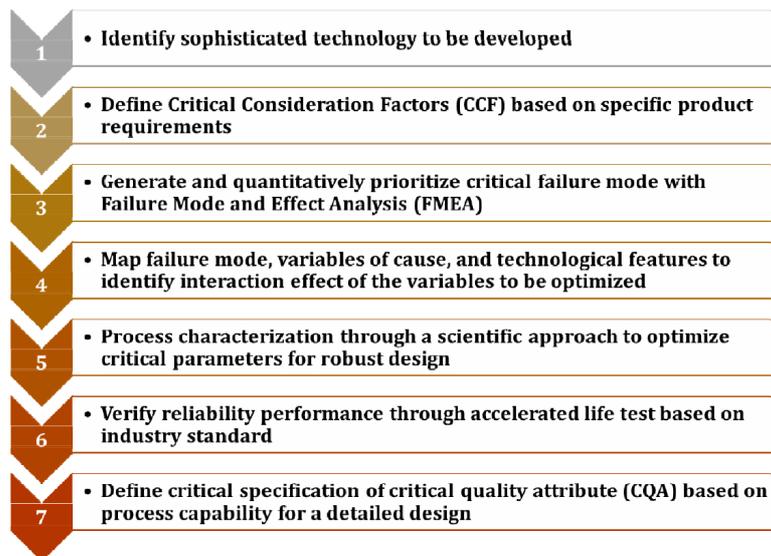
Figure 8. Overview of the development tools methodology

Figure 9. Elements of critical consideration factors

From the technical characteristics, all potential failure modes, with causative variables and quality attributes, can be identified. Risk priority can then be determined by utilizing the FMEA method. The complexity of emerging products generates large amounts of failure modes that must be accurately prioritized. Fuzzy logic is one of the most powerful tools in artificial intelligence (AI) to improve decision making concerning uncertain phenomenon, which is suitable to minimize the subjectivity of traditional FMEA. In this paper, fuzzy logic is used on the FMEA by integrating the new element of product lifetime (L) in addition to conventional severity (S), occurrence (O), and detectability (D) to calculate the modified risk priority number (RPN$_m$). Next, by setting a certain threshold, the failure mode can be classified based on risk level. As critical failure modes constitute the major concern that might hinder the adoption of new technology for mass production, their corresponding causative variables are then set to be the critical process parameter (CPP). The CPP needs to be managed through extensive process characterization in a scientific manner for robust design, and corresponding specifications need to be defined for a detailed design. Here, it is important to understand the relationship of the variables in the failure mode, as well as the correlated key technology features. Through critical parameter management (CPM), a robust system can be established by consistently employing the optimized parameters that fulfil the critical quality attribute (CQA) and reliability requirement throughout mass production. The result will also need to be well documented in an interconnected database network. Furthermore, with the advancement of Industry 4.0, a cyber-physical system (CPS) that connects digital and physical workflow allows for effective implementation of the robust system. This leads to realization of smart products that possess a high degree of autonomy in terms of its own operation, coordination and diagnosis, as the product has information/knowledge to understand itself, its environment, and its users throughout the lifecycle (Nunes, Pereira & Alves, 2017). With the proposed strategy, efficient implementation of new technology with minimum risk can be achieved to precisely fulfil the latest market niche in a timely fashion.

3. Implementation on the Proposed Technology

This section presents the implementation of the development tools in the development of the advanced substrate fabrication and surface finishing technology.

3.1. Critical Consideration Factor (CCF) Identification and Fuzzy Failure Mode and Effect Analysis (FMEA)

Figure 10 shows the flowchart of the CCF integration to FMEA, as well as CPM. To determine CCF, product requirements have to be fully understood according to the application by identifying the three elements presented in Figure 9. First, the technical characteristics must be defined based on the packaging requirements, i.e., the material, process, and design involved on each of the interfaces in the packaging configuration. Second, the expected lifetime of the product has to be identified to determine the necessary quality and reliability level, as shown in Figure 11 (Lee, Bieler, Kim & Ma, 2015). In this paper, high reliability products are targeted based on market needs. Finally, the yield requirement, which depends on the particular market and business model, have to be taken into account when determining the specifications. Defining CCF based on this can make a great difference in allocating development resources efficiently. With appropriate considerations, an efficient, yet accurate, development process can be achieved. First, the variables with resulting failure modes are determined based on the technical characteristics of the proposed technology. This is represented in the diagram in Figure 12.

These factors must be complete, as any items missed will emerge as failure modes in later stages entering mass production. Based on this diagram, a list of failure modes with causative variables and resulting quality attributes are presented in Appendix A. For a more precise failure mode risk prioritization, fuzzy logic is employed to address the subjectivity of traditional FMEA, and includes a new element of product lifetime (L). All of the ratings are given based on five experts from research and development (R&D), production engineering (PE), and quality assurance (QA) teams with at least 10 years of experience in the relevant area of expertise. First, the fuzzy linguistic variable is assigned based on a triangular fuzzy number (TFN) on each of the S, O, D, and L variables. The assignment description and membership function are shown in Tables 1 and 2 and Figures 13 and

14, respectively. Concerning the lifetime variable, the assignment is adjustable depending on the target product requirement. Here, the membership degree increases with lifetime, as we are targeting high reliability electronic products.
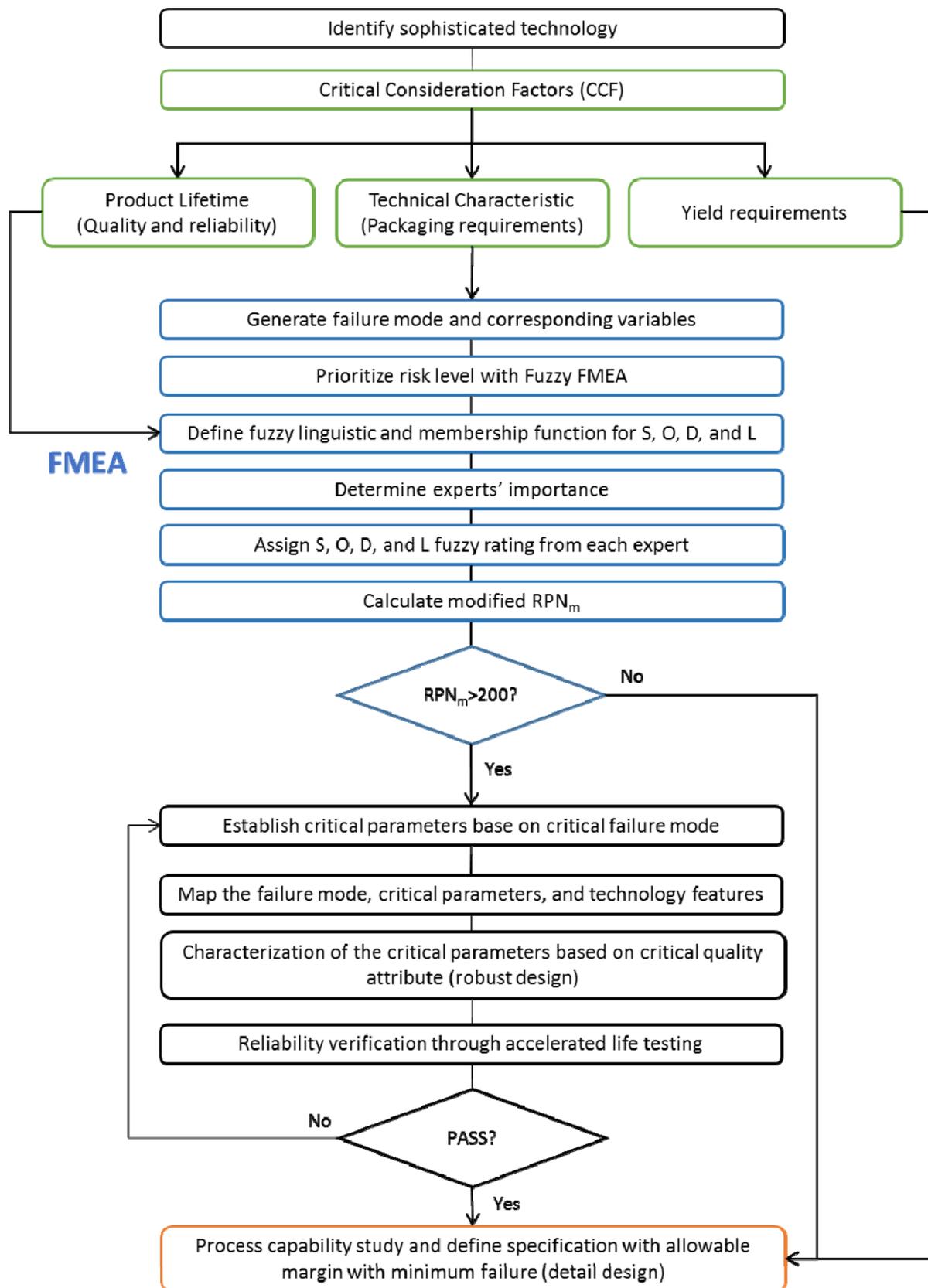
Figure 10. Flowchart on the implementation of the proposed development tools
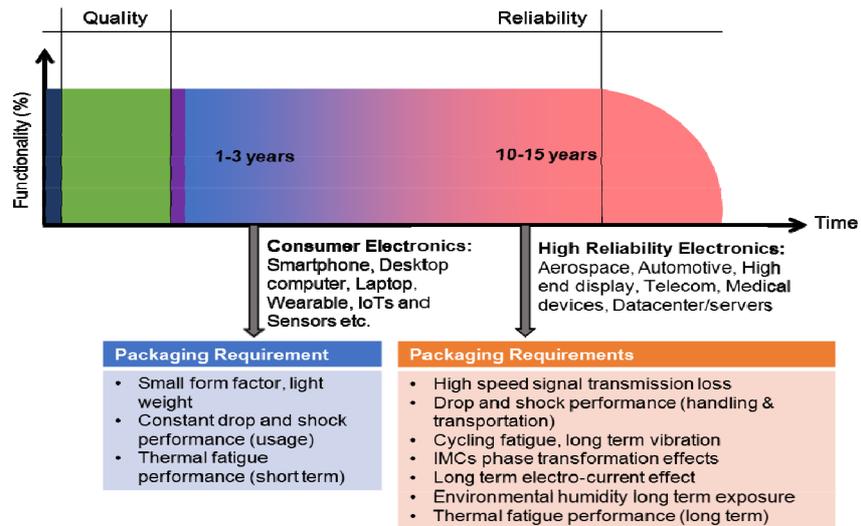
Figure 11. Quality and reliability considerations for consumer electronics and high reliability electronics (Lee, 2015)
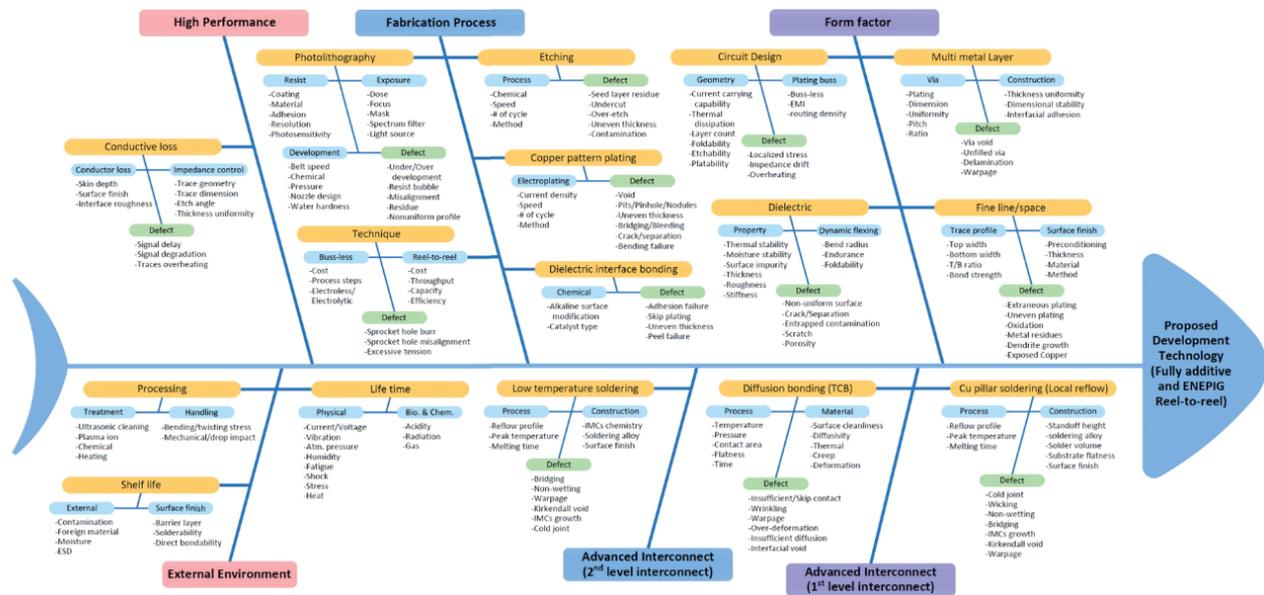
Figure 12. Factors and failure mode of the proposed technology development

Factors	Fuzzy linguistic terms				
Severity (S)	None (N)	Slight (Sl)	Moderate (Md)	High severity (HS)	Very high severity (VHS)
Occurrence (O)	Very low (VL)	Low (L)	Medium (M)	High (H)	Very high (VH)
Detection (D)	Extremely likely (EL)	High chances (HC)	Moderate chances (MC)	Low chances (LC)	Extremely unlikely (EU)
Fuzzy number	0,0,1.5	1,2.5,4	3.5,5,6.5	6,7.5,9	8.5,10,10

Table 1. Fuzzy linguistic variable assignment for S, O, and D
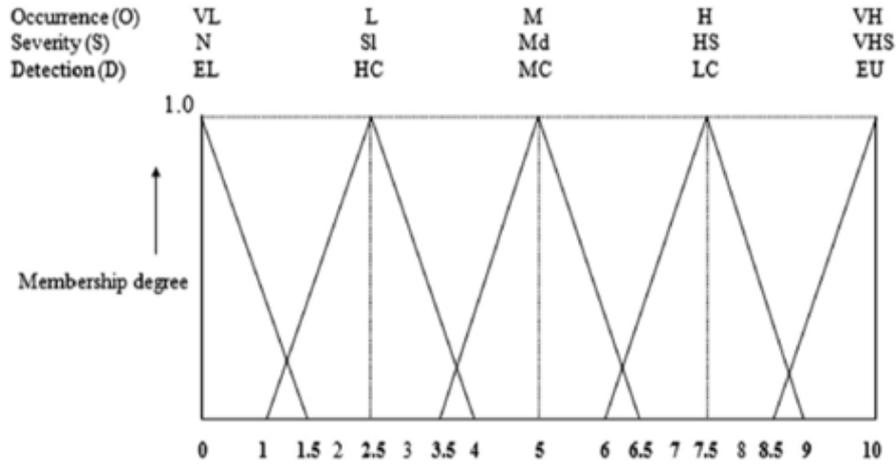
Figure 13. Fuzzy linguistic membership function for severity, occurrence, and detection (Kirkire, Rane & Jadhav, 2015)

Factors	Fuzzy linguistic terms		
Lifetime	Initial (I)	Short-term (ST)	Long-term (LT)
Fuzzy number	0,0,1/3	1/12,1/2,11/12	2/3,1,1

Table 2. Fuzzy linguistic variable assignment for L
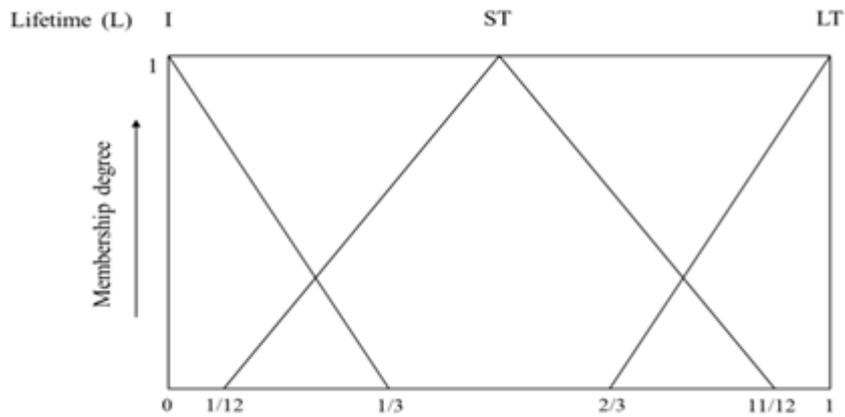
Figure 14. Fuzzy linguistic membership function for lifetime

The weight of experts that reflects their influence on the risk evaluation is then calculated using the following equation:

$$w_{tmk} = \frac{E_{tmk}}{\sum_{k=1}^{n} E_{tmk}} \tag{1}$$

where *tmk* is the *kth* team member; and E is the expertise. The weights of the experts are presented in the following table.

Team member	1	2	3	4	5
Weight	0.3	0.25	0.2	0.15	0.1

Table 3. Weight assignment of each team member

Assignment of the fuzzy linguistic variable is shown in Appendix B. The fuzzy linguistic terms are calculated based on the methodology developed by Kirkire et al (2015), as shown in the following:

$$S_{ij}^n = (SL_{ij}^n, SM_{ij}^n, SU_{ij}^n), S_{ij}^n \in T ,$$

where

$$0 \le SL_{ij}^n \le SM_{ij}^n \le SU_{ij}^n \le 10 \tag{2}$$

$$O_{ij}^n = (OL_{ij}^n, OM_{ij}^n, OU_{ij}^n), O_{ij}^n \in T ,$$

where

$$0 \le OL_{ij}^n \le OM_{ij}^n \le OU_{ij}^n \le 10 \tag{3}$$

$$D_{ij}^n = (DL_{ij}^n, DM_{ij}^n, DU_{ij}^n), D_{ij}^n \in T ,$$

where

$$0 \le DL_{ij}^n \le DM_{ij}^n \le DU_{ij}^n \le 10 \tag{4}$$

$$L_{ij}^n = (LL_{ij}^n, LM_{ij}^n, LU_{ij}^n), L_{ij}^n \in S ,$$

where

$$0 \le LL_{ij}^n \le LM_{ij}^n \le LU_{ij}^n \le 1 \tag{5}$$

$$S_{ij} = S_{ij}^1 \times W_{tm1} + S_{ij}^2 \times W_{tm2} + ... + S_{ij}^n \times W_{tmn} \tag{6}$$

$$O_{ij} = O_{ij}^1 \times W_{tm1} + O_{ij}^2 \times W_{tm2} + ... + O_{ij}^n \times W_{tmn} \tag{7}$$

$$D_{ij} = D_{ij}^1 \times W_{tm1} + D_{ij}^2 \times W_{tm2} + ... + D_{ij}^n \times W_{tmn} \tag{8}$$

$$L_{ij} = L_{ij}^1 \times W_{tm1} + L_{ij}^2 \times W_{tm2} + ... + L_{ij}^n \times W_{tmn} \tag{9}$$

Where S_{ij}^n, O_{ij}^n, D_{ij}^n and L_{ij}^n are the severity, occurrence, detectability, and lifetime, respectively, assigned by n experts for interface of i and risk of j; $S_{ij}^n \in T$, $O_{ij}^n \in T$, $D_{ij}^n \in T$ and $L_{ij}^n \in S$ are the membership function of the triangular fuzzy number S_{ij}, O_{ij}, D_{ij} respectively; L_{ij} is the severity, occurrence, detectability, and lifetime value of experts' opinion for interface i and risk j; W_{tmk} is the weight of kth team member; and n is the number of experts. Fuzzy numbers on the probability of $S, O, D,$ and L are aggregated by equations (6)-(9) (Lin, Liu, Liu & Wang, 2013). Next, these fuzzy numbers are defuzzified into numerical values by the following equation:

$$DS_k = \frac{[(SU_k - SL_k) + (SM_k - SL_k)]}{3} + SL_k \ \forall k \tag{10}$$

$$DO_k = \frac{[(OU_k - OL_k) + (OM_k - OL_k)]}{3} + OL_k \ \forall k \tag{11}$$

$$DD_k = \frac{[(DU_k - DL_k) + (DM_k - DL_k)]}{3} + DL_k \, \forall \, k \tag{12}$$

$$DL_k = \frac{[(LU_k - LL_k) + (LM_k - LL_k)]}{3} + LL_k \, \forall \, k \tag{13}$$

Where DS_k, DO_k, DD_k and DL_k are the defuzzified severity, occurrence, detectability, and lifetime fuzzy sets, respectively. Finally, the modified RPN can be calculated using the equation below:

$$RPN_m = DS_k \text{ x } DO_k \text{ x } DD_k \text{ x } DL_k \tag{14}$$

Based on this RPN_m, the failure mode is classified as follows: above 200 is set to be critical risk; between 100 to 200 is set to be moderate risk; between 50 to 100 is set to be low risk; and below 50 is set to be negligible risk. In this study, 19 critical failure modes have been identified out of a total of 61 failure modes (Figure 15).
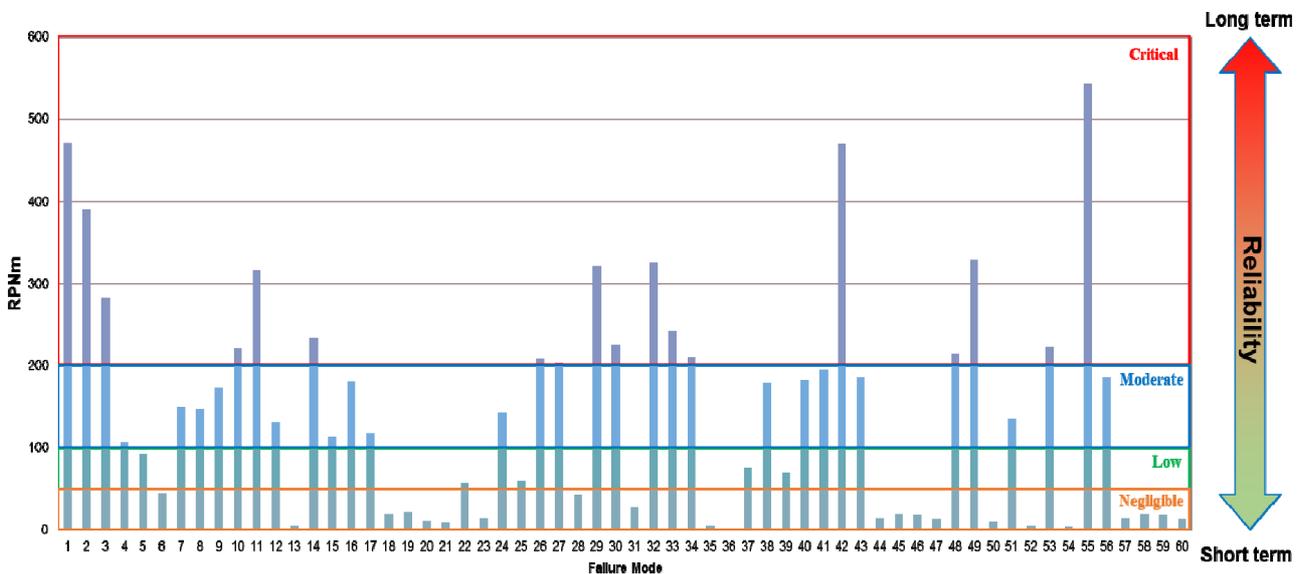
Figure 15. Failure mode RPN in the development of advanced flexible substrate

3.2. Process Characterization and Critical Parameter Management

After the critical failure modes have been determined, the critical parameters are then identified from the causative variables. The relationship between these failure modes, critical parameters, and technological features need to be accurately mapped to elucidate the influence and interaction of each parameter, as shown in Figure 16.
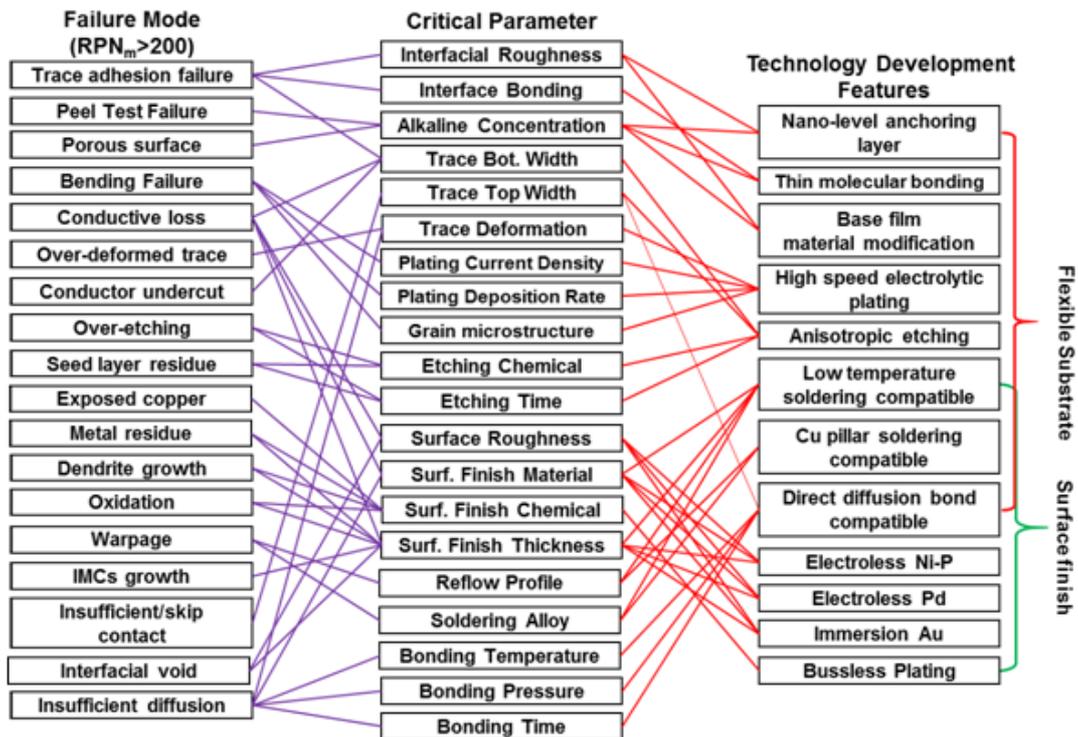
Figure 16. Correlation between high priority failure mode, critical parameter, and technology development features

The next step is to perform process characterization on each of the critical parameters to determine the optimal value so that a robust design of the system can be established. This characterization has to be performed with a scientific methodology with an appropriate design of experiment (DOE). For each DOE, the range of the critical parameter has to be first determined based on existing data or from the literature. Defining this is crucial, as a range that is too wide will cost more resources and unnecessarily lengthen the development time. The optimization result will be based on the resulting critical quality attribute, which is also quantified in-depth with the appropriate scientific tool. The scope of the optimization should also consider interaction effects between each variable to ensure that there are no contradicting failure modes that emerged from the same critical parameter. Table 5 presents the result of critical parameter optimization based on the critical quality attribute criteria for the development of reel-to-reel FAP and ENEPIG. All of the results from the DOE must also be included in the interconnected database. Determining the optimum critical parameters constitutes the core of this development strategy since it allows the system to produce the most desired result and consequently minimize or eliminate any failure mode to meet even the most demanding specifications of the critical quality attribute. Depending on the application, a product will have a certain window of acceptable CQA. Meeting this specification is typically quantified by Cpk as a process capability index, which describes the extent to which the mean of the process lies in the middle of the specification upper and lower limit. Essentially, the higher the Cpk, the better the system is capable of meeting the required specification, leading to a robust process. Figure 17 shows the consequence of a CPP that has not been properly optimized. It can be seen that with the same machine capability, there is still a chance/window for failure to occur when CPP is not optimized.
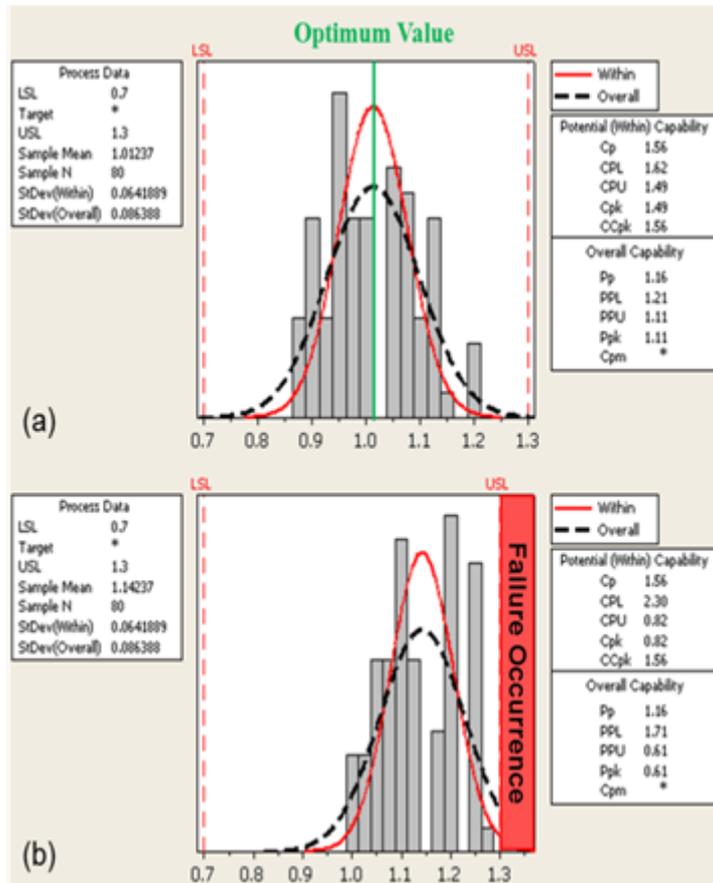
Figure 17. Process capability of trace top/bottom ratio (a) robust design with CPM and (b) uncontrolled system design with occurrence of failure
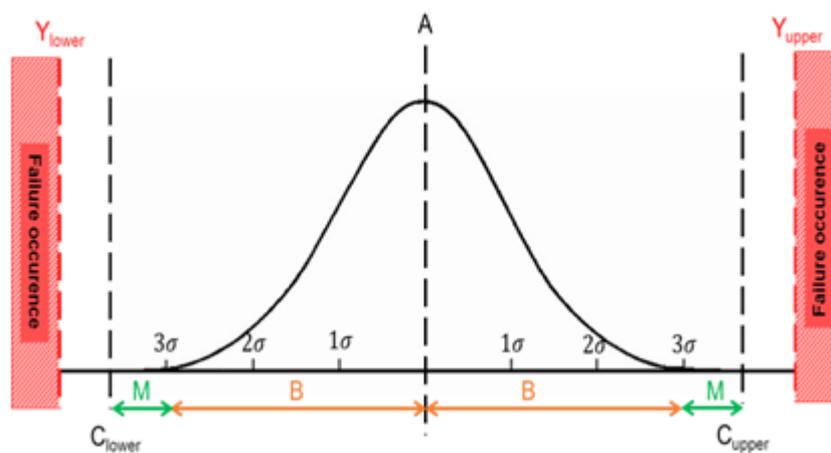
Figure 18. Detailed specification based on process capability

Technological Features	Fuzzy FMEA Sorted Failure Mode	Process Characterization					Reliability Verification (PASSED)	
		Parameter	Range Studied	Optimum Value	Parameter	Target	Condition	Method/ Tools
Metallurgy diffusion bond compatible (Pun, Dhaka, Cheung & Chan, 2017a)	Interfacial void	Temperature	180-340°C	320°C	Shear strength	>50 MPa	Temperature Humidity Storage (60°C/60% RH for 1000 h)	FIB cross-section
	Insufficient diffusion	Pressure	55-175 Mpa	155 Mpa				
	Insufficient/ skip contact	Time	1-11 s	10 s				
	Exposed copper	Ni Thickness	1-3 um	3.0 um	Trace peeled off (peel test failure mode)	100%		
	Metal residue	Pd Thickness	0.05-0.4 um	0.4 um	Bonding misalignment	<2 um	Thermal Shock Test (125°C to -40°C for 1000 cycles)	Electrical test
	Dendrite growth	Au Thickness	0.04-0.07 um	0.04 um	Void formation	Fully shrunk		
	Oxidation	Surface roughness (Ra)	90-150 nm	<100 nm				
Cu pillar micro bump(C2) compatible (Pun, Islam, Cheung & Chan, 2017b)	IMCs growth	Ni Thickness	1-1.3 um	1 um	Overall IMCs thickness after isothermal aging	<4 um	Thermal aging 150°C for 1000 h	SEM/EDX & cross-sectioning
	Exposed copper							
	Metal residue	Pd Thickness	0.05-0.4 um	0.05-0.2 um	Critical IMCs formed	$(Pd,Cu,Au)Sn_4$ $(Cu,Ni)_6Sn_5$		
	Dendrite growth	Au Thickness	0.04-0.2 um	0.04-0.07 um	Die peel failure interface	Within solder side		
	Oxidation				Growth rate constant of IMCs	$<2x10^{-14}$ cm^2/s		
Low temperature solder compatible (Sn-Bi-Ag) (Pun et al., 2018a)	IMCs growth	Ni Thickness	1-4 um	1-1.5 um	Shear strength	>1000 gf	Extended reflow at 175°C for 120 mins	SEM/EDX & cross-sectioning
	Exposed copper	Pd Thickness	0.04-0.7	0.15-0.2 um	Failure mode	100% solder on interface		
	Metal residue	Au Thickness	0.03-0.05 um	0.04 um	Critical IMCs formed	$(Ni,Cu)_3Sn_4$		
	Dendrite growth							
	Oxidation				Ni consumption	0.009 um/min reflow		
Base film modification and nano-level chemical bonding (Pun, Ali, Kohtoku, Cheung, Chan & Wong, 2018b)	Trace adhesion failure	Modifier concentration (on polyimide)	15-40 mL/L	25 mL/L	PAA layer thickness	<5 nm	Temperature Humidity Storage (85°/85% RH)	TEM inspection
					Carboxyl bonding	>3%	Low Temperature Storage (-40°C for 500 h)	XPS analysis
	Peel test failure				Amide bonding	>6%	Hight Temperature Storage (150°C for 500h)	
								Peel test

Technological Features	Fuzzy FMEA Sorted Failure Mode	Process Characterization					Reliability Verification (PASSED)	
		Parameter	Range Studied	Optimum Value	Parameter	Target	Condition	Method/ Tools
	Porous surface				Peel strength	>0.6 kN/m	Moisture Senstivity Level 3 (-60°C to 60°C for 48 h and 3x reflow at 254°C)	
	Signal delay/ propagation				Ni-P layer coverage	100%	Thermal Shock Test (125°C to -40°C for 500 cycles)	SEM inspection
					Thickness	100-110 nm		
High speed electrolytic pattern plating (Pun et al., 2018b)	Bending endurance failure	Plating rate	0.2-0.6 um/min	0.2 um/min	Grain size	>2 um	Heat treatment (200°C and 300°C for 24 h)	SIM cross-sectioning
		Current density	1-2.5 ASD	1 ASD	Bending endurance	>35 cycles		
	Over-deformed trace	Temperature	315-375°C	345°C	Strain	<0.2		
		Pressure	120-160 MPa	140 MPa	Interfacial microstructure of Au-Au	Interlocking nano-twin structure		
Isotropic etching (Pun et al., 2018b)	Conductor undercut	Etching time	60-75 s	75 s	Insulation resistance	>10^5 Ohms	Temperature Humidity Bias (85°C/85% RH/20 VDC)	Insulation resistance measurement
					Insulation resistance after thermal humidity bias	>10^5 Ohms		
	Over-etching				Standard deviation of impedance	<1		
					T/B ratio	~1		
					Cpk of T/B ratio	>1.33		
	Seed layer residue				Line/space scalability	<8/8 um		
					Cpk of line/space	>1.33		
Signal performance (Pun et al., 2018b)	Signal delay/ propagation	Interface roughness (Rq)	40-320 nm	40-70 nm	Conductor loss factor (Ksr)	<1.05	N/A	

Table 5. Critical parameter optimization based on the critical quality attribute criteria

After the process characterization, the optimal value and the acceptable process window with minimum failure can be obtained. For each critical parameter identified, the optimal value is further verified in terms of the reliability through the relevant accelerated life testing. Once the reliability is guaranteed, the optimal value is run on the production line to simulate high volume production. From this, the variation from unit-to-unit and batch-to-batch can be identified to determine the machine process capability. Depending on the target sigma level, the detail specification can be determined by fulfilling the following equations:

$$C_{upper} = (A+B) + M \tag{15}$$

$$C_{lower} = (A-B) - M \tag{16}$$

$$\left| C_{upper} - Y_{upper} \right| \geq \sigma, \; C_{lowerr} - Y_{lower} \geq \sigma \tag{17}$$

where A is the optimal value from process characterization; Y_{upper} and Y_{lower} are the upper and lower limit before the occurrence of failure, respectively; B is half of the target sigma level; C_{upper} and C_{lower} are the lower and upper specification, respectively; and M is the margin allowed for the specification as shown in Figure 18. Allowing this margin is crucial so that room for error exists, which means that even though the process is outside of the sigma level standard, failure will still not occur. Obviously, the margin should be adjusted depending on the process capability, targeted sigma level, and yield requirement.

Finally, the robust system has to be followed up by appropriate operational management practices so that the optimum design can be carried out consistently throughout production. Critical parameter management is one excellent practice to assure that system robustness is maintained through detail specification, proper documentation, and in line quality control (QC) (Clausing, Frey & Systems Engineering, 2010). With a manufacturing and production implementation plan for the critical parameters, quality evaluation, and changes in the control plan, the value created through robust design can be delivered to the customer.

4. Conclusion

Enabling robust technology transfer with minimum time-to-market constitutes the key to enhance business competitiveness in high tech enterprises. With increasing complexity and diversification of products to meet future market demands, a higher risk of failure is inevitable at the NPD stage. Field failure is particularly detrimental to manufacturers, as failure occurs on the customer's premise. This paper established a unique methodology of prioritizing critical failure mode by embedding the product long term reliability into consideration using fuzzy-based FMEA. The methodology is implemented on the development of advanced flexible substrate in the flexible electronics industry. It has been demonstrated that the methodology is capable of capturing the critical failure mode and consequently can be prevented through process characterization on the critical parameters. Finally, the reliability is also verified following the industry standard to ensure desirable and consistent performance throughout product lifetime. Therefore, a balanced ecosystem of innovation can be realized by ensuring that the value created through new product development is thoroughly captured by commercialization in a timely manner.

Declaration of Conflicting Interests

The authors declared no potential conflicts of interest with respect to the research, authorship, and/or publication of this article.

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Appendix

Appendix A. List of failure modes

Component	No.	Potential Failure Mode	Effect of Failure Mode	Causative Variables	Quality Attribute	Method of Detection	RPN_m	Risk Level
Base Film	1	Trace adhesion failure	Trace peeled off	Interfacial roughness	Bonding molecule composition	Surface profilometer	470.10	Critical
				Interface bonding mechanism	Anchoring layer thickness	XPS analysis on bond content		
				Trace geometry (bottom width)		Cross sectional analysis		
	2	Peel test failure	Trace peeled off	Alkaline concentration	Peel strength	Peel strength test	390.10	Critical
	3	Porous surface	Skip pattern build up	Alkaline concentration	Modification layer coverage	SEM inspection	282.53	Critical
	4	Entrapped contamination	Skip pattern build up	Chemical impurity level	Contaminant content	SEM/EDX analysis	106.35	Moderate
				Handling				
	5	Scratch	Open trace	Roller alignment	Scratch density	Visual inspection	91.46	Low
				Particle deposition				
				Handling				
						Electrical simulation		
	6	Crack/separation	Open trace	Reel tension	Crack/separation density	Visual inspection	44.26	Negligible
	7	Skip/uneven plating	Skip pattern build up	Chemical concentration	Exposed PI region	Visual inspection	149.71	Moderate
	8	Warpage	Open trace	Heat treatment profile	Surface flatness after reflow	Flatness measurement	146.95	Moderate

Component	No.	Potential Failure Mode	Effect of Failure Mode	Causative Variables	Quality Attribute	Method of Detection	RPN_m	Risk Level
				CTE mismatch				
	9	Non uniform surface morphology	Skip pattern build up	Incoming material defect	Surface defect density	SEM inspection	173.37	Moderate
			Incompatibility for high speed application					
Cu Metallization	10	Bending endurance failure	Trace crack	Current density	Bending cycle	Mandrel test	220.5	Critical
				Deposition rate	Bending cycle (annealed)	SEM inspection		
				Grain microstructure		FIB cross sectioning		
	11	Signal delay/propagation Conductive loss	Incompatibility for high speed application	Surface roughness (skin depth)	Loss factor	Surface profilometer	316.60	Critical
				Surface finish (material and thickness)		Electrical simulation		
				Trace undercut				
	12	Trace overheating	Trace crack	Operating current	Thermal dissipation rate	Thermal simulation	130.34	Moderate
				Trace surface area				
	13	Surface abnormities Pits/Pinhole/Nodules	Open/short circuit	Current density	Surface defect density	SEM inspection	5.09	Negligible
				Deposition rate				
				Chemical bath impurity				
	14	Over-deformed trace	Intermittent connection	Plastic deformation characteristic	Strain	Cross section analysis	233.30	Critical
						SEM inspection		
	15	Via micro-void	Signal integrity	Deposition rate	Void density	Cross section analysis	112.50	Moderate
				Residue	Void size			
	16	Non-Fully filled via	Signal integrity	Sidewall residue	Via volume	Cross section analysis	179.82	Moderate
				Polyimide melting				
	17	Uneven plating thickness	Not bondable surface	Residue deposit	Surface flatness	Surface profilometer	116.58	Moderate
				Skip seed layer plating				
	18	Broken via sidewall	Open circuit	Metallization integrity	Sidewall defect	Electrical test	19.40	Negligible
	19	Bridging (bleeding)	Short circuit	Resist adhesion	Insulation resistance	Electrical test	21.60	Negligible
Photolithography	20	Resist bubbles	Open/short circuit	Coater air entrapment	Resist surface defect	Visual inspection	11.37	Negligible
				Lamination temperature				
				Lamination pressure				

Component	No.	Potential Failure Mode	Effect of Failure Mode	Causative Variables	Quality Attribute	Method of Detection	RPN_m	Risk Level
				Lamination time				
	21	Under/over development	Open/short circuit	Resist thickness uniformity	Resist opening width	Visual inspection	9.18	Negligible
				Exposure time				
	22	Residue deposition	Open traces	Chemical bath impurity	Residue content	SEM inspection	56.94	Low
	23	Exposure Misalignment	Open/short circuit	Sprocket hole damage	Alignment	Visual inspection	13.57	Negligible
	24	Non-uniform profile (Feet Protrusion)	Trace peeled off	Exposure energy source	Resist feet dimension	SEM inspection	142.49	Moderate
				Exposure energy dose	T/B ratio			
				Resist material				
Seed layer removal	25	Chemical contaminant	Solder resist adhesion	Chemical bath impurity	Contaminant content	Tape test	58.38	Low
	26	Conductor undercut	Trace peeled off	Trace geometry (bottom width)	T/B ratio	FIB cross sectioning	208.36	Critical
	27	Over-etching	Impedance deviation	Etching chemical	Impedance consistency	Cross sectioning	203.20	Critical
				Etching time	Line/space			
	28	Uneven thickness	Trace crack	Etching chemical	Surface flatness	Visual inspection	42.11	Negligible
	29	Seed layer metal residue	Short circuit	Etching chemical	Insulation resistance	Insulation resistance measurement	321.48	Critical
				Etching time	Insulation resistance (after aging)			
Surface Finishing	30	Exposed copper	Corrosion	Plating chemical	Copper coverage	SEM/EDX analysis	224.99	Critical
	31	Extraneous plating	Short circuit	Plating thickness	Surface finishing coverage	Visual inspection	27.40	Negligible
	32	Metal residue	Short circuit	Plating thickness	Insulation resistance	SEM inspection	325.36	Critical
	33	Dendrite growth	Short circuit		Insulation resistance	Accelerated aging test	242.18	Critical
	34	Oxidation	Open trace	Plating chemical	Oxide content	Accelerated aging test	209.44	Critical
						XPS analysis		
Reel-to-reel with buss-less technique	35	Sprocket hole burr	Open/short circuit	Punching pressure	Sprocket hole dimension	Visual inspection	4.50	Negligible
				Punching tool residue				
	36	Sprocket hole misalignment	Wrong registration	Punching misprogram	Registration accuracy	Visual inspection	1.87	Negligible
	37	Excessive tension	Broken film	Roller speed mismatch	Mechanical defect	Visual inspection	74.95	Low
				Film thickness				
Circuit Design	38	Localized stress	Trace cracking	Geometry changes	Bending location	Bend test	178.98	Moderate

Component	No.	Potential Failure Mode	Effect of Failure Mode	Causative Variables	Quality Attribute	Method of Detection	RPN_m	Risk Level
	39	Impedance drift	Signal degradation	Trace dimension	Impedance consistency	Impedance measurement	70.07	Low
	40	Overheating	Trace cracking	Thermal dissipation area	Thermal dissipation rate	Thermal simulation	182.32	Moderate
				Signal current				
Copper Pillar Soldering (1st level interconnect)	41	Warpage	Open solder joint	Reflow profile	Surface flatness after reflow	Visual inspection	194.52	Moderate
				Soldering alloy		Electrical test		
	42	IMCs growth	Brittle joint	Surface finish (thickness)	IMCs thickness	Cross sectioning	469.27	Critical
				UBM consumption rate	Critical IMCs	SEM/EDX analysis		
					IMCs growth rate	Accelerated aging test		
					Die peel failure mode			
	43	Kirkendall void	Joint reliability	Surface finish (thickness)	Void dimension	Cross sectioning	184.85	Moderate
				Reflow profile		SEM inspection		
	44	Bridging	Short circuit	Solder volume	Soldering spacing	Electrical test	13.96	Negligible
	45	Non-wetting	Open joint	Surface contamination	Contaminant content	Electrical test	19.46	Negligible
	46	Cold joint	Open joint	Reflow profile	Melted solder volume	Electrical test	17.59	Negligible
				Soldering alloy				
	47	Wicking	Open joint	Reflow profile	Gold plating coverage	Electrical test	13.30	Negligible
				Surface finish				
Thermo-compression Bonding (1st level interconnect)	48	Insufficient contact/skip contact	Open joint	Trace contact area (top width)	Alignment offset	X-ray inspection	213.25	Critical
	49	Interfacial void	Joint reliability	Surface finish (thickness)	Void formation	FIB cross sectioning	328.67	Critical
				Surface roughness				
	50	Substrate warpage	Trace crack	Reflow peak temperature	Substrate flatness	Flatness measurement	9.90	Negligible
				Reflow ramp rate				
	51	Over-deformation	Trace crack	Bonding pressure	Strain	Cross sectioning	134.97	Moderate
						SEM inspection		
	52	Wrinkling	Trace crack	Bonding temperature	Substrate flatness	Visual inspection	4.34	Negligible
	53	Insufficient diffusion	Joint reliability	Surface finish (metal diffusivity)	Interface microstructure	Cross sectioning	221.67	Critical
				Bonding temperature				

Component	No.	Potential Failure Mode	Effect of Failure Mode	Causative Variables	Quality Attribute	Method of Detection	RPN_m	Risk Level
				Bonding pressure	Peel test failure mode	SEM inspection		
				Bonding time				
Low Temperature Soldering (2nd level interconnect)	54	Substrate Warpage	Open solder joint	Reflow peak temperature	Surface flatness after reflow	Flatness measurement	3.43	Negligible
				Reflow ramp rate				
	55	IMCs growth	Joint reliability	Surface finish (thickness)	IMCs thickness	Cross sectioning	543.70	Critical
					Critical IMCs formed	SEM inspection		
					Shear strength			
					Shear failure mode	Accelerated aging test		
					UBM consumption rate			
	56	Kirkendall void	Joint reliability	Surface finish (thickness)	Void dimension	X-ray inspection	184.85	Moderate
				Reflow profile				
	57	Bridging	Short circuit	Solder volume	Soldering spacing	Electrical test	13.96	Negligible
	58	Non-wetting/solder skip	Open joint	Surface contamination	Contaminant content	Electrical test	19.46	Negligible
	59	Cold joint	Open joint	Reflow profile	Melted solder volume	Electrical test	17.59	Negligible
				Soldering alloy				
	60	Wicking	Open joint	Reflow profile	Gold plating coverage	Electrical test	13.30	Negligible
				Surface finish				

Appendix B. Evaluation of severity, occurrence, detection, and lifetime by experts using fuzzy linguistic terms

Factors	Team Member	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
S (Severity)	TM1	VHS	HS	HS	HS	SI	VHS	HS	HS	HS	HS	Md	SI	VHS	SI	Md	HS	VHS	VHS	HS	VHS	HS	VHS	Md	Md	HS	VHS	Md	HS	HS	HS
	TM2	VHS	VHS	HS	Md	Md	HS	HS	HS	Md	HS	Md	HS	HS	VHS	Md	Md	Md	VHS	VHS	HS	VHS	HS	Md	Md	VHS	VHS	Md	HS	HS	HS
	TM3	VHS	VHS	HS	VHS	Md	HS	HS	HS	Md	Md	HS	Md	Md	VHS	SI	HS	HS	VHS	HS	VHS	VHS	VHS	HS	HS	SI	HS	HS	HS	VHS	VHS
	TM4	VHS	VHS	Md	HS	SL	VHS	HS	HS	HS	Md	HS	HS	HS	VHS	Md	Md	Md	VHS	VHS	VHS	VHS	VHS	Md	Md	HS	SI	VHS	HS	HS	VHS
	TM5	VHS	VHS	HS	VHS	Md	HS	HS	HS	HS	Md	HS	HS	HS	VHS	Md	Md	Md	VHS	VHS	VHS	VHS	HS	HS	HS	SI	VHS	HS	Md	HS	VHS
O (Occurrence)	TM1	VH	H	H	H	H	M	H	M	M	H	VH	VH	H	H	H	M	H	L	H	H	H	H	VH	VH	M	VH	H	L	H	M
	TM2	M	VH	M	H	L	M	L	L	M	VH	VH	H	H	H	M	M	M	H	L	VH	VH	VH	VH	VH	H	H	H	L	M	M
	TM3	VH	M	M	H	L	M	L	L	M	H	H	H	H	M	M	M	M	L	VH	VH	VH	H	H	H	VH	VH	H	VH	H	H
	TM4	VH	H	H	VH	H	M	M	M	M	H	VH	H	H	VH	H	M	L	H	M	VH	VH	H	VH	VH	M	VH	H	M	H	M
	TM5	M	H	H	M	H	L	M	L	H	VH	VH	H	M	M	L	H	H	H	M	VH	VH	H	H	H	M	H	VH	L	M	H
D (Detection)	TM1	LC	LC	LC	LC	LC	HC	LC	EU	LC	MC	MC	MC	EL	MC	LC	LC	MC	EL	MC	EL	EL	EL	EL	MC	LC	MC	MC	LC	EU	MC
	TM2	MC	MC	EU	MC	EU	EL	LC	HC	LC	MC	MC	MC	EL	HC	LC	LC	LC	HC	HC	EL	EL	HC	MC	HC	MC	HC	HC	LC	EU	MC
	TM3	EU	MC	EU	MC	EU	EL	EU	EU	MC	MC	MC	HC	EL	MC	LC	MC	LC	HC	HC	HC	EL	MC	HC	MC	EU	MC	HC	EL	LC	EU
	TM4	LC	LC	LC	LC	LC	HC	EU	HC	LC	EU	EU	MC	EL	MC	LC	EU	HC	MC	HC	HC	HC	HC	EL	MC	MC	MC	MC	LC	EU	LC
	TM5	MC	EU	EU	LC	EU	EL	EU	HC	LC	HC	EU	MC	EL	MC	LC	LC	MC	EL	HC	HC	HC	HC	EL	HC	LC	HC	MC	MC	EU	LC
L (Lifetime)	TM1	LT	LT	LT	I	ST	LT	LT	LT	LT	LT	LT	ST	ST	LT	LT	LT	LT	I	I	I	I	I	ST	I	LT	ST	LT	LT	ST	LT
	TM2	LT	LT	ST	ST	ST	LT	ST	LT	ST	LT	LT	ST	I	LT	LT	ST	ST	I	I	I	I	I	ST	ST	ST	I	ST	ST	ST	ST
	TM3	LT	LT	LT	ST	LT	ST	ST	LT	ST	LT	LT	ST	I	ST	LT	ST	ST	I	ST	I	I	ST	ST	ST	I	LT	LT	LT	ST	ST
	TM4	LT	LT	LT	I	ST	ST	ST	LT	ST	LT	LT	LT	ST	LT	ST	LT	ST	I	ST	I	I	I	I	I	ST	I	LT	I	ST	ST
	TM5	LT	LT	ST	I	ST	LT	LT	ST	LT	LT	LT	ST	I	ST	LT	ST	LT	ST	ST	I	I	ST	I	ST	I	LT	ST	ST	I	ST

Factors	Team Member	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60
S (Severity)	TM1	VHS	VHS	HS	HS	HS	VHS	VHS	HS	HS	HS	HS	VHS	HS	HS	VHS	VHS	HS	HS	VHS	HS	HS	HS	Md	SI	Md	SI	HS	N	VHS	Md
	TM2	VHS	HS	HS	VHS	HS	VHS	VHS	HS	Md	HS	VHS	HS	HS	VHS	VHS	HS	HS	VHS	HS	HS	HS	Md	SI	SI	SI	HS	HS	VHS	VHS	HS
	TM3	VHS	HS	Md	HS	HS	VHS	HS	HS	Md	HS	VHS	HS	Md	HS	VHS	VHS	VHS	HS	VHS	Md	Md	Md	SI	SI	N	HS	Md	VHS	VHS	VHS
	TM4	VHS	HS	HS	HS	HS	VHS	HS	HS	HS	Md	HS	Md	HS	Md	VHS	VHS	HS	VHS	VHS	Md	SI	SI	SI	HS	N	VHS	Md	VHS	VHS	VHS
	TM5	VHS	VHS	HS	HS	HS	HS	VHS	HS	HS	Md	HS	Md	HS	HS	VHS	VHS	HS	HS	HS	HS	HS	Md	SI	SI	HS	HS	VHS	VHS	HS	VHS
O (Occurrence)	TM1	H	M	H	VH	L	L	M	M	H	M	H	VH	M	M	M	H	H	H	H	H	H	H	M	M	VH	M	M	M	H	H
	TM2	VH	H	M	H	VL	L	M	H	H	M	H	VH	H	L	H	H	H	VH	H	H	M	VH	M	M	H	H	H	H	H	VH
	TM3	VH	H	H	H	VL	M	M	H	VH	L	VH	H	L	H	H	H	H	VH	H	H	M	VH	M	M	H	L	H	H	H	H
	TM4	H	M	H	VH	L	M	H	H	H	M	VH	VH	M	H	H	H	H	VH	H	H	M	VH	M	M	VH	M	M	H	M	H
	TM5	H	M	M	H	L	M	H	M	H	L	H	H	H	L	L	H	VH	M	H	H	VH	M	H	H	H	H	L	M	H	H
D (Detection)	TM1	EL	LC	MC	MC	HC	EL	MC	MC	MC	EU	MC	EU	LC	EL	EL	EL	EL	HC	EU	HC	MC	EL	EU	HC	EU	LC	EL	EL	EL	EL
	TM2	HC	LC	MC	HC	EL	LC	LC	LC	EU	MC	LC	EU	EU	EL	HC	HC	HC	MC	EU	HC	LC	HC	EU	HC	EU	EL	HC	HC	HC	HC
	TM3	EL	MC	LC	HC	MC	EL	LC	LC	MC	MC	HC	EU	LC	MC	MC	MC	HC	MC	EU	HC	MC	EL	EU	HC	EU	LC	MC	MC	MC	HC
	TM4	EL	LC	LC	MC	MC	EL	MC	MC	MC	MC	EU	LC	MC	MC	MC	EL	MC	EU	HC	LC	EL	HC	EU	HC	LC	MC	LC	MC	MC	HC
	TM5	HC	EU	MC	HC	HC	EL	MC	MC	MC	LC	HC	EU	EU	EL	EL	MC	EL	MC	EU	HC	LC	HC	EU	HC	EU	EU	EL	EL	MC	EL
L (Lifetime)	TM1	I	LT	LT	LT	I	I	I	ST	I	LT	LT	LT	LT	I	I	I	I	LT	LT	I	LT	I	LT	I	LT	LT	I	I	I	I
	TM2	ST	LT	LT	ST	I	I	I	ST	I	LT	LT	LT	LT	I	I	I	I	LT	LT	I	LT	I	LT	I	LT	LT	I	I	I	I
	TM3	ST	LT	LT	LT	I	I	ST	LT	ST	LT	ST	ST	LT	I	I	I	ST	LT	I	ST	LT	I	LT	I	ST	ST	I	I	I	I
	TM4	I	LT	LT	ST	I	I	ST	LT	ST	ST	I	LT	ST	I	I	I	I	LT	I	ST	I	LT	I	LT	ST	I	I	I	I	I
	TM5	I	LT	LT	LT	I	I	I	ST	ST	ST	ST	LT	ST	I	I	I	I	ST	LT	I	LT	I	LT	I	LT	ST	I	I	I	I